
ABSTRACT

A Leakage power dissipation is becoming a concern in field-programmable gate arrays (FPGAs) due to scaling in FPGA technology. Field programmable gate arrays (FPGAs) are the implementation platform of choice when it comes to design flexibility. However, the high power consumption of FPGAs (which arises due to their flexible structure), make them less appealing for extreme low power applications hence it is important to investigate ways of reducing FPGA power consumption. This paper proposes an energy efficient dual-threshold CarbonNanotube Field Effect Transistor (CNFET) based architecture of 4-input Look-up Table (LUT), a building block of Field programmable gate arrays. HSPICE simulation based on Berkeley Predictive Technology Model (BPTM) for 32nm channel length, in the CNFET based LUT delay is improved by 95% and is 98% more leakage power efficient than the LUT implemented in the bulk CMOS.

KEYWORDS: FPGA, CNFET, LUT

INTRODUCTION

Leakage power dissipation has been an area of concern in CMOS technology for some time now. Leakage power dissipation occurs as a result of undesirable currents flowing through the CMOS transistors when they are scaled down. With scaling, it is now possible to have FPGAs with a high density of devices. As many of these devices sit idle for long periods of time, they contribute to increased static power dissipation that is mainly caused due to leakage currents. Leakage power dissipation has grown to be a significant fraction of overall chip power dissipation in modern processes and it is expected to grow significantly in future processes [1], [2]. Due to increasing complexity of modern digital designs and because of low NRE (non recurring engineering) cost and short time to market, field programmable gate arrays (FPGAs) have become an attractive implementation option [3]. FPGA's use much more transistors per function than application specific integrated circuits to achieve programmability resulting in higher leakage power consumption [4]. Most of the early work on low power FPGA's was focused on dynamic power consumption, but, now leakage power has become almost 50% of the total FPGA power [5]. FPGA's consist of an array of logic blocks that are connected through the routing switches. The logic blocks are composed of LUT's and flip-flops [6], [7]. FPGA block diagram is shown in figure 1 below. Most of the research work till now is concentrated on reducing the leakage within the routing switches, which accounts for more than 60% of total FPGAs leakage [8]. The leakage power of LUT which currently comprises ~25% of total chip power, has also become equally important with the advent of new commercial FPGA's such as Altera's Stratix-III and Xilinx Vertex-5 which uses larger LUT [9], [10].

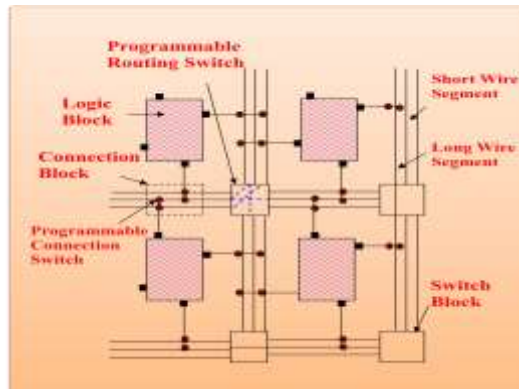


Figure 1: Block Diagram of FPGA

This paper explores the subthreshold performance of novel devices for FPGA based LUT in deep submicron 32nm technology node for ultra low power applications. In this paper we have implemented a 4-input LUT in Carbon nanotube based field effect transistor (CNFET) technology. Due to superior conductance, very high ION/IOFF ratio, high drive current and high thermal stability, CNFET will be the best choice to minimize the leakage power in future FPGA's [9].

LOOK-UP TABLE

The basic 3-input LUT structure is shown in Figure 1. This is similar to the traditional LUT design [9]. The output of the LUT is connected to one of 8 SRAMs through a path that is controlled by pass gates. The 8 SRAMs store the logic function of the LUT. Each input turns on exactly one path between some SRAM cell and the output. The number of stages in the LUT is equal to the number of inputs of the LUT, as depicted in Figure 1. The stages are labeled in Figure 2. In general, a larger number of inputs of the LUT is desired as it gives the LUT the ability to be configured with a more complex logic function. The increased number of stages required as the number of inputs of the LUT increases, causes an increase in the number of pass gates the signals must propagate through before they can appear at the output. In our design, we chose an NMOS pass gate-based LUT instead of a CMOS pass gate-based LUT, because the extra PMOS device in the CMOS pass gate will increase area and capacitance, thus degrading its performance and area efficiency as was shown in [9]. However, in super-threshold operation, the use of an NMOS pass gate-based LUT results in a drop in the output voltage of the first stage by threshold voltage V_T . This can be corrected by the use of a restoring buffer P at the output, yielding a full voltage swing at the output. The output of the inverter P is connected to both a flip-flop and a MUX. The MUX chooses between a non-registered versus a registered output of the LUT. The output of the MUX is then regenerated by means of a low-switching point inverter Q connected to a PMOS keeper, as shown on the right of Figure 2.

The whole LUT circuitry is implemented in the regular threshold voltage (R_{vt}). Fig. 3 shows the circuit of level restoring buffer here the transistors MN1 and MP2 which are critical for the rising signal transition are implemented in regular threshold voltage (R_{VT}), while MP1 and MN2 implemented in high threshold voltage. With this balanced rising and falling technique, compared to base-line level restoring buffer, a delay penalty of only 11% with substantial 69% and 64% reduction in active and standby leakage respectively have been achieved[2]. All the Mux Tree transistors have regular threshold voltage on account of high delay penalty by using high threshold voltage H_{VT} for these transistors.

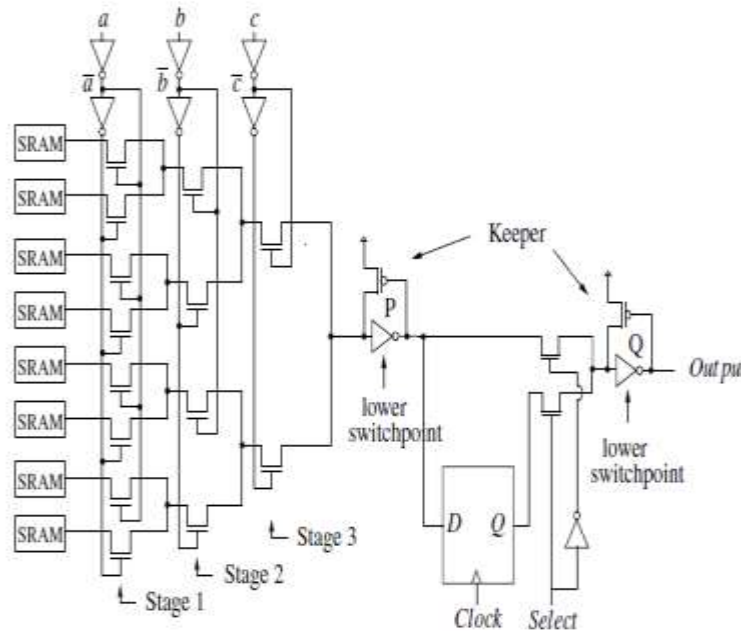


Figure 2: 3 input LUT

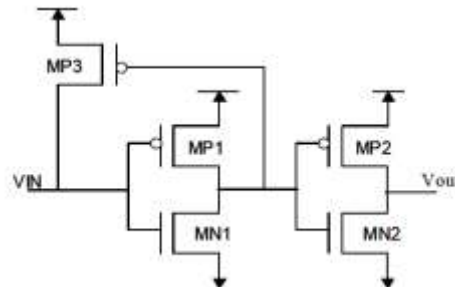


Figure 3: Level Restoring Buffer

To achieve high integration density CMOS semiconductor devices are scaled aggressively. But leakage power dissipation and variability are the drawbacks of scaling. To overcome these drawbacks of scaling we use CNFET technology for LUT in next section.

PERFORMANCE ANALYSIS USING CNFETS CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Carbon Nanotube Field Effect Transistor

The research community actively investigates CNFETs as a promising device for integrated circuit technology at the end or beyond the ITRS roadmap. The most promising devices among emerging technologies is CNFET. Most of the fundamental limitations for traditional MOSFETs are reduced in CNFETs. The single wall carbon nanotube (SWCNTs) is one-dimensional conductor obtained by sheets of graphene rolled in the form of tubes. Fig. 4 shows a CNFET structure. It has a similar structure as MOSFET. It has a structure that has bulk dielectric material on top of silicon substrate and uses SWNT as the channel. Depending on the structure, SWNT will have either metallic or semiconducting property. This property is described by the chiral vector (n, m), where n and m are integers of some vector equation. When the difference between n and m is either 0 or a multiple of 3's, SWNT has metallic property,

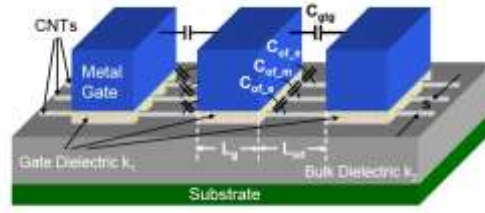


Figure 4: 3D CNFET Structure

Furthermore, the chiral vector influences the diameter of SWNT. The diameter of CNT is given by equation (1),

$$D_{CNT} = \frac{a\sqrt{m^2 + n^2}}{\pi} \quad (1)$$

Where m, n are chirality number of CNT, ‘a’ is the Lattice constant ($a=2.49e^{-10}$). The Threshold voltage of CNFET is given by equation [9],

$$V_{TH} = \frac{\sqrt{3}}{3} \frac{aV\pi}{D_{CNT}} \quad (2)$$

Where, $V\pi = 3.03q$ is the carbon PI-PI bond energy.

Dual Threshold CNFET based LUT

We implement dual threshold 4-input LUT using CNFET similar as shown in figure 2. using MOSFET. The band-gap E_g of CNFET depends strongly on its diameter (d) as $E_g \cong \Delta/d$, thus for conduction to start, the barrier at the source channel has to overcome $E_g/2=\Delta/d$. By changing the diameter of CNT we can vary the threshold voltage (V_T) of CNFET because the barrier height determines the threshold potential of CNFET therefore $V_{th} = \Delta/d$, hence this approach is used to boost V_T by 0.1v, so as to consider high threshold voltage (Hvt) transistor throughout this text, this can be achieved by selecting the chiralities (13,0) for simulation. Hence we use chirality (13,0) for level restoring buffer and chirality (19,0) is used for LUT circuitry for simulation. Table below shows performance comparison Dual V_T and Single V_T CNFET LUT. Dual V_T CNFET LUT gives 62% improvement in power and 65% improvement in delay.

Table 1. Comparison of single V_T and dual V_T CNFET LUT

Sr no	Parameter	Single V_T CNFET LUT	Dual V_T CNFET LUT
1.	Average power	1.90nW	0.72nW
2.	Delay	0.44ps	0.15ps

To evaluate the performance benefit of CNFET for FPGAs a dual threshold CNFET LUT is implemented in bulk and CNFET transistors at 32nm technology. The selected (W/L) ratio for NMOS and PMOS transistors is 2 and 4 respectively. Similarly a (19, 0) chirality of CNFET each with 3 nanotubes for N and P CNFET is considered over here for comparison. Similarly the level restoring buffer of respective LUT is sized up in terms of width and number of CNTs. Simulation is carried out at frequency of 770MHz with supply voltage ranging from 0.2 V TO 0.4 V. delay

and power of both LUT is observed shown in table 2 and 3.

Table 2. Delay Comparison of CMOS and CNFET LUT

Vdd	CMOS LUT delay(ns)	CNFET LUT delay(ns)
0.2	201	2.02
0.25	92	0.9
0.3	51.1	0.54
0.35	30.5	0.19
0.4	20	0.086

Table 2. Comparison of power consumed by CMOS and CNFET LUT

Vdd	CMOS LUT power(nW)	CNFET LUT power(nW)
0.2	10.4	0.5
0.25	17	0.75
0.3	27.7	0.69
0.35	43.5	1.04
0.4	68.6	1.34

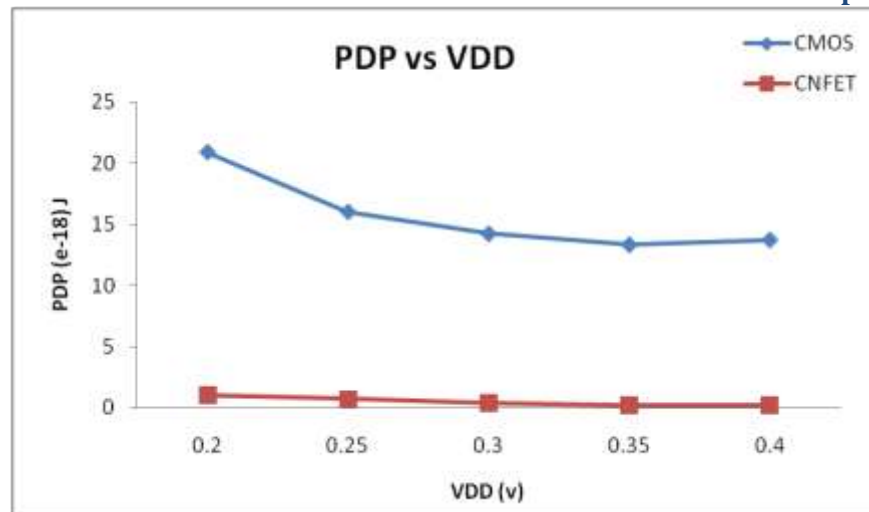


Figure 5: PDP as function of supply voltage

Due to higher mobility and ballistic transport of CNFET, the LUT implemented with CNFET has high speed shown in Table 2. Similarly the effective width of CNFET is very small therefore switching power consumption of CNFET LUT is lower than bulk LUT shown in Table 3. Due, to lower delay and power consumption the PDP of CNFET LUT is lower than that of implemented in bulk. As the parasitic load of LUT circuit is high therefore for higher V_{DD} range (from 0.2V to 0.4V) the PDP decreases, thereafter for lower V_{DD} (i.e. at '0.2V') the delay increases abruptly and PDP also increased. This is due to longer critical path of 4- input LUT (i.e. 16:1 multiplexer which is sub-block of LUT). The optimum PDP obtained for both LUT is at $V_{DD}=0.4V$. Due to advantage of lower power consumption and higher speed of CNFET, the CNFET based LUT provides 97% improvement in optimum PDP compared to CMOS LUT as depicted in Figure 5.

CONCLUSION

In this paper 32nm bulk and CNFET based technology is used to evaluate the leakage performance of 4-input Look-up Table. Based on HSPICE simulation we find that by using dual threshold CNFET based LUT power is improved by 62% and delay improved by 65% compared to single threshold CNFET based LUT. CNFET based LUT are 98% more leakage power efficient and delay is improved by 95% than the LUT implemented in the bulk technology. Due to advantage of lower power consumption and higher speed of CNFET, the CNFET based LUT provides 97% improvement in optimum PDP compared to CMOS LUT as depicted in Figure 5. This shows that CNFET holds a lot of promise as an alternative to the MOS transistor for implementing future low power FPGAs logic blocks.

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